Reducing Costs Through Thermal Simulation

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Stacked modules are becoming increasingly popular, with thermal management being a critical consideration in most stacked module applications because of their power density. We take a look at a specific case in which a stacked module had to be developed for a critical defence application. Thermal simulations on the initial concept design highlighted the defects of the design and enabled engineers to select the least expensive potting compound that would meet the thermal requirements of the application.

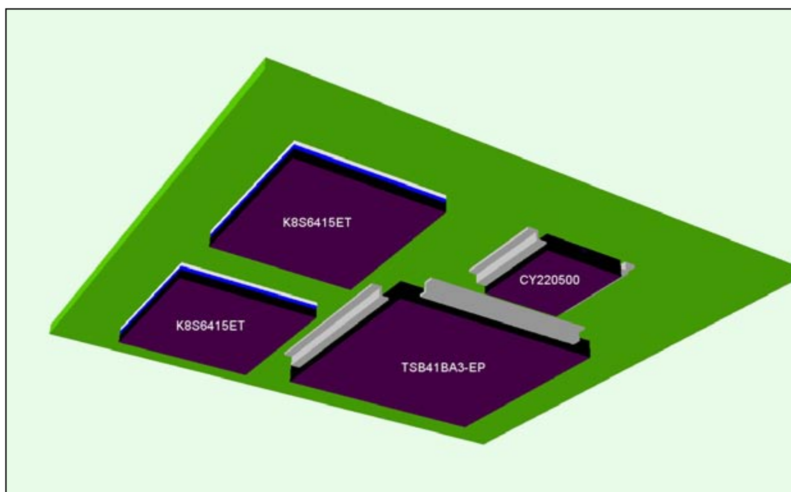
C-Mac MicroTechnology, an electronics design and manufacturing company based in South Denes, Great Yarmouth, United Kingdom, recently developed a stacked module for a critical defence application. Prior to building prototypes, C-Mac engineers performed thermal simulation on the initial concept design and discovered that junction temperatures on the module ranged up to 125°C, well above the 100°C maximum. They realised they needed a potting compound to reduce thermal resistance and wanted to select the least expensive formulation that would meet the thermal requirements of the application.

Simulating the junction temperatures of the devices in the stacked modules while using three different potting compounds, it was discovered that the thermal requirements of the application could be met with a potting compound that cost only one-half as much as the highest-performing potting compound. Simulation was much faster and less expensive than the alternative of building and testing prototypes.

Type	Part No.	Qty	Package	PWR (W)
SoC	ASIC	1	Bare Die	2.80
IEEE1394	TSB41BA3	1	PQFP-80	2.00
SDRAM	K4T51163QE	2	FBGA-84	0.40
NORFlash	K8S6415EBB	2	FBGA-44	0.20
PLL	CY22050F1	3	TSSOP-16	0.25

Table 1 – The eight packaged devices of the module used in this application

Figure 1 – Upper PCB



Thermal design challenge

Stacked modules are becoming increasingly popular as system complexity and packing density increases. Thermal management is a critical consideration in most stacked module applications because of their power density. The critical task from a thermal standpoint is removing the heat from within the stack so it can be dissipated by external heatsinks. The module used in this application incorporates eight packaged devices, one bare die and two printed circuit boards (PCBs) as detailed in Table 1.

The module is constructed of a ball grid array (BGA) lower PCB with some of the SMD components and an inverted upper PCB with the remaining devices. The module is partitioned so as to separate the higher power components and maintain signal integrity. Figures 1 and 2 show the upper and lower halves of the model respectively. The interconnect required between top and bottom PCBs is made via edge connections with support between the two PCBs provided by a kovar ring frame. The highest power dissipating component, the SoC ASIC is placed on the lower PCB while the next highest – the TSB41BA3 – is mounted on the upper PCB in a diagonally opposite corner. This makes it possible for heat to be transferred out of either or both the upper or lower surfaces.

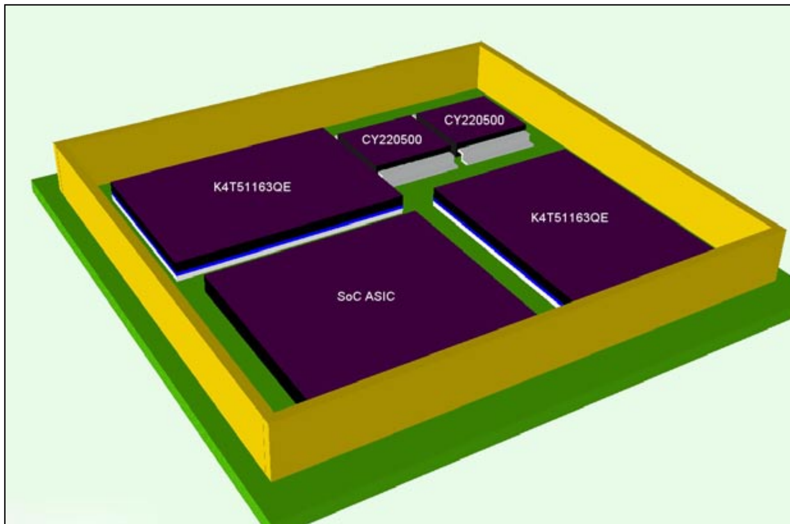


Figure 2 – Lower PCB

Table 2 – Cost vs. performance of representative potting compounds

Compound type	Relative cost	Thermal conductivity (W/m.K)
Standard	1	0.3
Enhanced	1.5	0.6
Best	3	1.3

Simulation streamlines design process

A thermal simulation was performed at C-Mac on the initial design using FloTherm computational fluid dynamics (CFD) software from the Mentor Graphics Mechanical Analysis Division (formerly Flomerics). FloTherm is used because it provides many tools that reduce the time required to model complex stacked module designs. For C-Mac, the most important of these tools is the FloThermPack web-based wizard which quickly produces accurate models of integrated circuits and other components.

The modelling process was begun by gathering information on component package styles and power dissipations as shown in Table 1. Some of these estimated power dissipations are based on typical datasheet values under known conditions. FloTherm was then used to generate a conceptual model by defining the dimensions and the substrate, underfill and cavity materials. The model of discrete cuboids was constructed with material properties, most importantly thermal conductivity, assigned to each.

The FloThermPack web-based wizard was used to generate models of each of the components. It would have taken a considerable amount of time to define the geometry of each of these components to the level required to obtain accurate junction temperature predictions. Using the FloThermPack wizard, however, it was only necessary to enter basic design parameters such as the die size, die flag size and lead frame clearance. FloThermPack generated models of the components that were almost there. Only minor modifications had to be made, such as removing some extra balls on the BGAs and changing the thermal conductivity of the PCBs and the model was ready to be inserted. With FloThermPack, C-Mac engineers were able to model this stacked module in less than half the time that would have been required using conventional modelling methods.

Next the size of the cells in the model were defined, using smaller grid cells in areas where more detail was needed such as the higher powered components. The environment in which the module is mounted in the end application was also defined. At this early stage in the design process, it was necessary to make some assumptions. These included mounting the module on an infinite heatsink with the temperature held at 70°C.

The simulation results for the initial concept design showed that junction temperatures were much too high, up to 125°C. The obvious next step was to try a potting compound to reduce the thermal resistance of the module and conduct heat from the devices more readily to the heatsink. There are a number of different potting compounds available. As a general rule, as the thermal conductivity of the potting compound rises the cost also rises. The goal was to find the least expensive potting compound that would maintain junction temperatures of all of the devices on the board safely within the 100°C design specification.

Identifying the optimal thermal solution

The traditional method to address this goal would have been to build prototypes and run physical experiments with each type of potting compound, but it would have

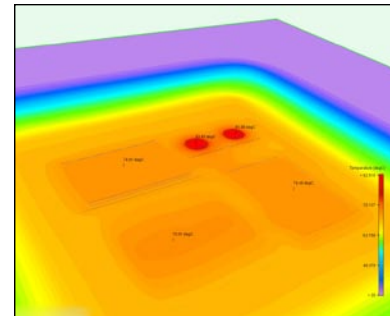
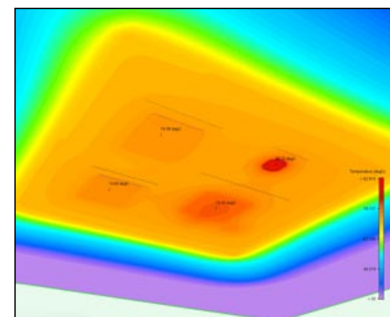


Figure 3 – Horizontal slice through lower PCB

Figure 4 – Horizontal slice through upper PCB



Compound type	Simulated junction temperature
Standard	110°C
Enhanced	85°C
Best	75°C

Table 3 – Simulation results of various potting compounds

taken a considerable amount of time and money to build prototypes, assemble them with different types of potting compounds and run physical tests. The hardest part would have been measuring the junction temperature of the different devices.

Thermal simulations of the stacked module were run with three different potting compounds which are called here: standard, enhanced and best. Table 2 shows the relative thermal performance and cost of the three potting compounds. For example, the table shows that the best potting compound has approximately four times the thermal conductivity and is three times as expensive as the standard potting compound.

Figures 3, 4, 5 and 6 show the temperatures predicted by the simulation for the enhanced potting compound. Figures 3 and 4 show the scalar isotherm planar plots of the lower and upper PCBs respectively. There are two hotspots on the lower PCB at approximately 92°C caused by two phase lock loop (PLL) devices. There are also two hotspots on the upper PCB produced by another PLL at 88°C and the TSB41BA3 device also at 88°C.

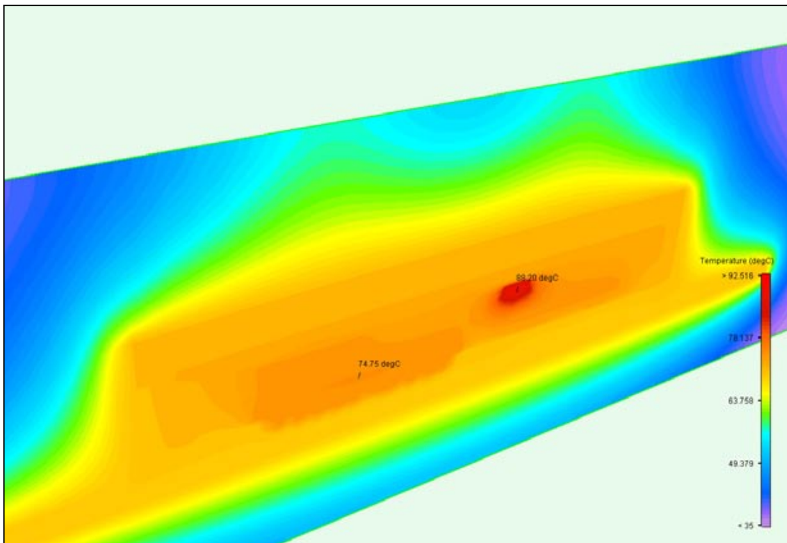
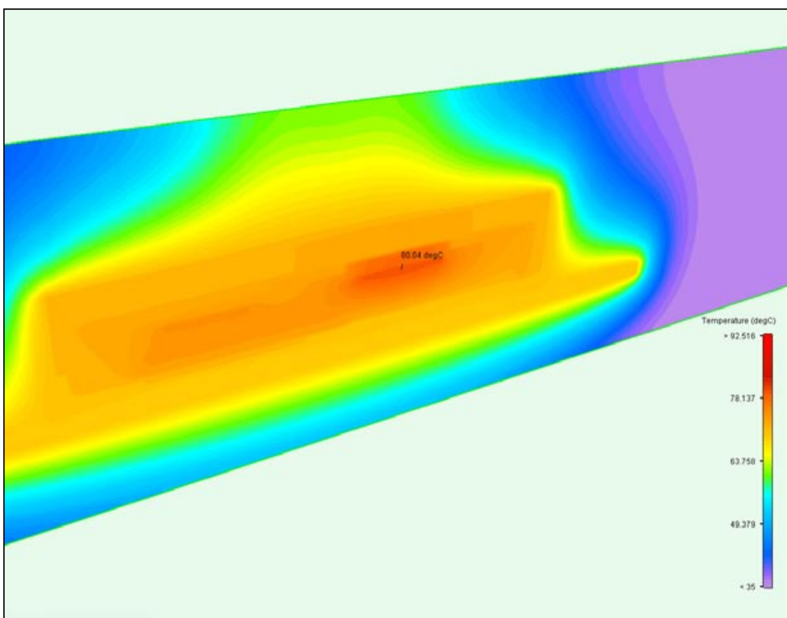


Figure 5 – Vertical slice through module (position 1)
Figure 6 – Vertical slice through module (position 2)



Figures 5 and 6 show two vertical cross-sections through the module. The cross-section in Figure 5 is positioned to show the PLL device on the upper PCB and the SoC and associated thermal balls on the lower PCB. Figure 6 takes a slice through the IEEE1394 device on the upper PCB and the SDRAM on the lower PCB. The figures indicate that temperatures within the module are fairly uniform, reflecting the high thermal conductivity of the best potting compound. The lines on the figures where colours change from one shade to another represent temperature gradients that indicate areas of higher thermal resistance. The hotspots in the images are centred around the junctions of the higher-powered and/or higher thermal resistance components in the module. Note that none of the components exceeds the design specification of 100°C.

The performance of all three potting compounds was simulated. The results are summarised in Table 3. The simulation demonstrated that both the enhanced and best potting compounds brought the core temperature down to acceptable levels with ample safety margin on the die junction temperatures. So engineers at C-Mac were able to specify the enhanced potting compound at a cost of about half of the best potting compound. Without simulation C-Mac engineers would have been faced with two unattractive alternatives. They could have undertaken a much lengthier and more expensive physical testing process to identify the potting compound that provided the best mix of performance price. Or they could have foregone this process and used the best potting compound because we were fairly confident that it would have delivered acceptable thermal performance. Thermal simulation, on the other hand, gave the best of both worlds by identifying an optimised solution while minimising engineering costs and leadtime.